Abstract Submitted
for the MAR14 Meeting of
The American Physical Society

Thermionic charge transport in CMOS nano-transistors[1] ANDREAS BETZ, M. FERNANDO GONZALEZ ZALBA, Hitachi Cambridge Laboratory (UK), SYLVAIN BARRAUD, CEA-LETI (France), QUENTIN WILMART, BERNARD PLACAIS, Laboratorie Pierre Aigrain (France), DAVID A. WILLIAMS, Hitachi Cambridge Laboratory (UK) — We report on DC and microwave electrical transport measurements in silicon-on-insulator CMOS nano-transistors at low and room temperature. At low source-drain voltage, the DC current and AC response show signs of quantization with an additional dependence on back-gate bias. We attribute the quantization to Coulomb blockade resulting from barriers formed under the spacer regions of the chip. We show that at high bias transport occurs thermionic over the highest barrier: Transconductance traces obtained from microwave scattering parameter measurements can be accurately fitted by a thermionic model. From this we deduce the ratio of gate capacitance and quantum capacitance $C_g/C_q = C_{ox}/(C_{ox} + C_q)$, as well as the electron temperature T_e. We show that transport in our devices remains thermionic at high bias up to room temperature.

[1]Supported by the European Community 7th Framework and TOLOP

M. Fernando Gonzalez Zalba
Hitachi Cambridge Laboratory

Date submitted: 15 Nov 2013 Electronic form version 1.4