

MAR14-2013-005210

Abstract for an Invited Paper
for the MAR14 Meeting of
the American Physical Society

A graphene solution to conductivity mismatch: spin injection from ferromagnetic metal/graphene tunnel contacts into silicon

OLAF VAN 'T ERVE, Naval Research Laboratory

New paradigms for spin-based devices, such as spin-FETs and reconfigurable logic, have been proposed and modeled. These devices rely on electron spin being injected, transported, manipulated and detected in a semiconductor channel. This work is the first demonstration on how a single layer of graphene can be used as a low resistance tunnel barrier solution for electrical spin injection into Silicon at room temperature. We will show that a FM metal / monolayer graphene contact serves as a spin-polarized tunnel barrier which successfully circumvents the classic metal / semiconductor conductivity mismatch issue for electrical spin injection. We demonstrate electrical injection and detection of spin accumulation in Si above room temperature, and show that the corresponding spin lifetimes correlate with the Si carrier concentration, confirming that the spin accumulation measured occurs in the Si and not in interface trap states. An ideal tunnel barrier should exhibit several key material characteristics: a uniform and planar habit with well-controlled thickness, minimal defect / trapped charge density, a low resistance-area product for minimal power consumption, and compatibility with both the FM metal and semiconductor, insuring minimal diffusion to/from the surrounding materials at temperatures required for device processing. Graphene, offers all of the above, while preserving spin injection properties, making it a compelling solution to the conductivity mismatch for spin injection into Si. Although Graphene is very conductive in plane, it exhibits poor conductivity perpendicular to the plane. Its sp^2 bonding results in a highly uniform, defect free layer, which is chemically inert, thermally robust, and essentially impervious to diffusion. The use of a single monolayer of graphene at the Si interface provides a much lower RA product than any film of an oxide thick enough to prevent pinholes (1 nm). Our results identify a new route to low resistance-area product spin-polarized contacts, a crucial requirement enabling future semiconductor spintronic devices, which rely upon two-terminal magnetoresistance, including spin-based transistors, logic and memory.