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Towards parallel, CMOS-compatible fabrication of carbon nanotube single electron transistors MUHAMMAD ISLAM, DAEHA JOUNG, SAIFUL KHONDAKER, Department of Physics, Nanoscience Technology Center, University of Central Florida — We demonstrate an approach for the parallel fabrication of single electron transistor (SET) using single-walled carbon nanotube (SWNT). The approach is based on the integration of individual SWNT via dielectrophoresis (DEP) and deposition of metal top contact. We fabricate SWNT devices with a channel length of 100 nm and study their electron transport properties. We observe a connection between the SET performance and room temperature resistance (R_T) of the devices. Majority (90%) of the devices with $100 \text{ K}\Omega < R_T < 1 \text{ M}\Omega$, show periodic, well defined Coulomb diamonds with a charging energy around 15 meV, corresponding to transport through a single quantum dot (QD), defined by the top contact. For high R_T ($>1\text{M}\Omega$), devices show multiple QD behaviors, while QD was not formed for low R_T ($<100 \text{ K}\Omega$) devices. This easy, simple and CMOS-compatible fabrication process will provide a much desired insight towards the wide spread application and commercialization of SWNT SET devices.

Muhammad Islam
Department of Physics, Nanoscience Technology Center,
University of Central Florida

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