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Imaging of the native inversion layer in Silicon-On-Insulator wafers via Scanning Surface Photovoltage: Implications for RF device performance DAMINDA DAHANAYAKA, IBM Microelectronics, ANDREW WONG, Dartmouth College, PHILIP KASZUBA, LEON MOSZKOWICZ, JAMES SLINKMAN, IBM Microelectronics, IBM SPV LAB TEAM — Silicon-On-Insulator (SOI) technology has proved beneficial for RF cell phone technologies, which have equivalent performance to GaAs technologies. However, there is evident parasitic inversion layer under the Buried Oxide (BOX) at the interface with the high resistivity Si substrate. The latter is inferred from capacitance-voltage measurements on MOSCAPs. The inversion layer has adverse effects on RF device performance. We present data which, for the first time, show the extent of the inversion layer in the underlying substrate. This knowledge has driven processing techniques to suppress the inversion.

> James Slinkman IBM Microelectronics

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