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Thermoelectric power factor enhancement with electrically gated silicon nanowires BENJAMIN CURTIN, EMILIO CODECIDO, JOHN BOWERS, Univ of California - Santa Barbara — We present both an experimental and theoretical study of the thermoelectric properties of electrically gated silicon nanowires. In this work, conduction electrons are induced in Si nanostructures using an electrical gate instead of the typical ionized impurities, which strongly scatter charge carriers at doping densities necessary for optimal power factor. Eliminating ionized impurities results in increased mobility and is expected to improve the thermoelectric power factor. We explore the gate and geometry dependence of thermoelectric properties with a semi-classical, multi-subband Boltzmann transport model. A maximum power factor of $\sim 7 \times 10^3$ W/m-K^2 was calculated for Si NWs with cross-sectional areas between 6 nm and 8 nm, which corresponds to a 2x enhancement over bulk Si. We also discuss the effects of surface roughness, quantum confinement, and transport orientation on power factor. Tri-gated Si NWs with dimensions of 25 nm x 35 nm were also fabricated from silicon-on-insulator substrates and their power factor was determined for various gate biases. Power factor was found to increase monotonically with gate bias and reached a maximum value of $\sim 2.2 \times 10^3$ W/m-K^2, which slightly larger than a 40 nm thick and optimally doped n-type Si thin-film. We present the thermoelectric characterization of these gated Si NWs and provide physical explanations for several effects observed during measurements. We also discuss the potential for further power factor enhancement with smaller diameter Si NWs.

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