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Charge Offset Stability in Si Single Electron Devices with Al Gates M.D. STEWART, JR., National Institute of Standards and Technology, CHIH-HWAN YANG, NAI SHYAN LAI, WEE HAN LIM, ANDREW DZURAK, University of New South Wales, NEIL ZIMMERMAN, National Institute of Standards and Technology — The charge offset drift (time stability) is an important real-world issue in single electron devices (SEDs). For use as current standards for electrical metrology, we require time stability over long periods of time. For use as qubits, we require time stability for device integration and because, on short timescales, the charge offset drift can contribute to dephasing. Recently, workers have shown excellent qubit performance using aluminum gates on bulk Si wafers [1]. We report on the charge offset drift in these devices: the value (0.15 e) is intermediate between that of Al/AlO_x/Al tunnel junctions (greater than 1 e) and Si SEDs defined with Si gates (0.01 e). This range of values suggests that defects in the AlO_x are the main cause of the charge offset drift instability.

[1] J. J. Pla, K. Tan, J. Dehollain,W. Lim, J. Morton, D. Jamieson, A. Dzurak, and A. Morello, Nature 489, 541 (2012).

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