Abstract Submitted
for the MAR14 Meeting of
The American Physical Society

Tuning the gate efficiency in epitaxially grown InGaAs-InAs heterostructures[1] C.J. PALMSTRØM, Department of Electrical and Computer Engineering, UC Santa Barbara, J. SHABANI, California NanoSystems Institute, UC Santa Barbara — Fabrication of gate-defined devices on epitaxially grown heterostructures containing InAs layers is highly desirable as it offers the possibility of tuning the confinement potential, carrier density and spin orbit coupling. However, reliable gating has proven difficult in these materials due to gate leakage and hysteretic behavior. In addition, charge traps and Fermi level pinning could screen the applied electric field and significantly reduce the gate efficiency. In this work, we have studied the effect of surface gating on epitaxially grown $In_{0.75}Ga_{0.25}As$-InAs-$In_{0.75}Ga_{0.25}As$ quantum wells. We find that the application of the gate bias barely changes the carrier density and the efficiency of the gate to be poor. However when a positive voltage is applied to the gate during cool down, the gate efficiency is improved. Furthermore, the change in density as a function of gate bias becomes linear and the slope matches closely to the simple capacitance model. We have also fabricated a quantum point contact using a split gate design on a similar structure and achieved full depletion under the gates. The conductance plot as a function of side gate voltages shows quantized plateaus reminiscent of ballistic one-dimensional transport.

[1]A portion of this work was performed at the National High Magnetic Field Laboratory, which is supported by NSF Cooperative Agreement No. DMR-1157490, the State of Florida, and the U.S. DOE.

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Date submitted: 15 Nov 2013 Electronic form version 1.4