Abstract Submitted
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Graphene junction field-effect transistor TZU-MIN OU, TOMOKO BORSA, BART VAN ZEGHBROECK, Univ of Colorado - Boulder — We have demonstrated for the first time a novel graphene transistor gated by a graphene/semiconductor junction rather than an insulating gate. The transistor operates much like a semiconductor junction Field Effect Transistor (jFET) where the depletion layer charge in the semiconductor modulates the mobile charge in the channel. The channel in our case is the graphene rather than another semiconductor layer. An increased reverse bias of the graphene/n-silicon junction increases the positive charge in the depletion region and thereby reduces the total charge in the graphene. We fabricated individual graphene/silicon junctions as well as graphene jFETs (GjFETs) on n-type ($4.5\text{x}10^{15}$ cm^{-3}) silicon with Cr/Au electrodes and 3μm gate length. As a control device, we also fabricated back-gated graphene MOSFETs using a 90nm SiO_2 on a p-type silicon substrate (10^{19} cm^{-3}). The graphene was grown by APCVD on copper foil and transferred with PMMA onto the silicon substrate. The GjFET exhibited an on-off ratio of 3.75, an intrinsic graphene doping of $1.75\text{x}10^{12}$ cm^{-2}, compared to $1.17\text{x}10^{13}$ cm^{-2} in the MOSFET, and reached the Dirac point at 13.5V. Characteristics of the junctions and transistors were measured as a function of temperature and in response to light. Experimental data and a comparison with simulations will be presented.

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