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Enhanced Valley Splitting for Quantum Electronics in Silicon

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Silicon is a placid environment for quantum degrees of freedom with long spin and valley coherence times [1]. A natural drawback is that the same features that protect the quantum state from its environment also hamper its control with external fields. Indeed, engineered nanostructures typically lead to sub-meV splittings between valley states [2], hindering the implementation of both spin [1] and valley [3] based quantum devices. We will discuss the microscopic theory of valley splitting [2,4], presenting three schemes to control valleys on a scale higher than 1 meV: a) in a quantum well, the adoption of a barrier constituted of a layered heterostructure might lead to constructive reflection if the layer thicknesses match the electron wavelength, in analogy with a Bragg mirror [5]; b) the disparity between the high valley splitting in a impurity donor potential and the low splitting in a Si/Insulator interface may be harnessed controlling the tunneling between these two states, so that the valley splitting may be controlled digitally [6]; c) intrinsic Tamm/Shockley interface states might strongly hybridize with conduction states, leading to a much enhanced valley splitting[4], and its contribution to the 2DEG ground state may be experimentally identified [7]. We argue that this effect is responsible for the enhanced splitting in Si/BOX interfaces [8].

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