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3-D simulation of triple gate tunnel field effect transistor for enhanced transconductance and low sub-threshold swing NURUNNAHAR ISLAM MOU, MASSOOD TABIB-AZAR, University of Utah — Tunnel field effect transistors (TFET) are among emerging candidates with good sub-threshold swing (SS) much lower than the thermal limit of 60 mV/dec. TFET is a gated P^+-I-N^+ diode operated in reverse bias mode to use band-to-band tunneling as the working principle. However, low on-current and dependence of SS on gate voltage remain problematic prohibiting practical application of TFETs. Optimized device performance depends on many factors such as device geometry, gate geometry, choice of gate oxide and source region material, doping concentration etc. [1]. We present a 3-D simulation study of a triple gate all silicon TFET structure and evaluate the performance of the device for enhanced transconductance. In the simulated device, the gate wraps the channel region from three sides and hence the name triple gate. SS was optimized as functions of source and drain doping concentration, device thickness, width as well as different source and channel material system. Gate length scaling is also explored to enable further insight into affects of scaling on the device performance.

[1] Ionescu, A. M. & Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **479**, 329–337 (2011)

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