Abstract Submitted
for the MAR14 Meeting of
The American Physical Society

Low subthreshod swing tunnel field-effect transistor with two gated intrinsic regions YUYING ZHANG, MASSOOD TABIB-AZAR, Department of Electrical and Computer Engineering, University of Utah — We demonstrate a novel silicon tunnel field-effect-transistor (TFET), based on a reverse-biased p+-p-n-n+ structure, instead of the conventional p-i-n structure. The device was built on an ultrathin silicon body, SiO_2 and HfO_2 were used as gate dielectric. When positive gate voltage was applied to the n region, and negative gate voltage was applied to the p region, carriers accumulated at the surface of these two regions. Thus, the barrier width between them was reduced, and the conduction band of the n region became lower than the valence band of the p region. When the p+ region (source) was grounded and positive voltage was applied to the n+ region (drain), band-to-band tunneling (BTBT) took place at the p-n junction. 2D device simulations were performed by using Sentaurus Device. For the devices with SiO_2 gate dielectric, when V_{DS} =0.1 V, the subthreshold swing was 20 mV/decade. In this case, the subthreshold swing would increase with larger V_{DS}. The devices with HfO_2 gate dielectric had a subthreshold swing as low as 9.58 mV/decade, when V_{DS} was between 0.1 V and 0.5 V. Therefore, this silicon TFET with two gated intrinsic regions is a promising candidate for low power applications and fast switching.

Yuying Zhang
Univ of Utah

Date submitted: 03 Jan 2014 Electronic form version 1.4