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**Gate bias stress-induced threshold voltage instability of exfoliated multi-layer MoS<sub>2</sub> field effect transistors** KYUNGJUNE CHO, WOANSEO PARK, TAE-YOUNG KIM, TAKHEE LEE, Seoul Natl Univ — Recently, MoS<sub>2</sub> has attracted great attention due to its intriguing electrical properties. MoS<sub>2</sub> transistors with a high on/off ratio of 10<sup>8</sup> have recently been demonstrated using HfO<sub>2</sub> as the top gate dielectric [1]. Despite the merits of MoS<sub>2</sub>, large variations in the properties of MoS<sub>2</sub> FET devices due to extrinsic effects may result in limitations in device applications. Here, we investigated the gate bias stress effects of exfoliated multi-layered MoS<sub>2</sub> FETs. We observed that when a positive gate bias stress was applied to the device, the current decreased and the threshold shifted in the positive gate bias direction and vice versa. The electrical instability of the MoS<sub>2</sub> FETs was influenced by the measurement conditions. These phenomena can be explained by the charge trapping due to the adsorption or desorption of oxygen and/or water on the MoS<sub>2</sub> surface with a positive or negative gate bias, respectively, under an ambient environment. Our study will be helpful in understanding the electrical-stress-induced instability of the MoS<sub>2</sub>-based electronic devices [2].

[1] B. Radisavljevic et al., Nat. Nanotechnol. 6, 147(2011).

[2] K. Cho et al., ACS Nano, 7, 7751(2013).

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