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Topological Properties of Some Integrated Circuits for Very Large Scale Integration Chip Designs[1] S. SWANSON, M. LANZEROTTI, Augsburg College, G. VERNIZZI, J. KUJAWSKI, A. WEATHERWAX, Siena College — This talk presents topological properties of integrated circuits for Very Large Scale Integration chip designs. These circuits can be implemented in very large scale integrated circuits, such as those in high performance microprocessors. Prior work considered basic combinational logic functions [1] and produced a mathematical framework based on algebraic topology for integrated circuits composed of logic gates [2]. Prior work also produced an historically-equivalent interpretation of Mr. E. F. Rent's work for today's complex circuitry in modern high performance microprocessors, where a heuristic linear relationship was observed between the number of connections and number of logic gates [2]. This talk will examine topological properties and connectivity of more complex functionally-equivalent integrated circuits. References: [1] E. Hiteshue, K. Irvin, M. Lanzerotti, G. Vernizzi, J. Kujawski, A. Weatherwax, "Topological Properties of Basic Combinational Logic Functions for Very Large Scale Integrated Circuits," in 2014 Proc. APS Mtg., Denver, CO, 2014. [2] G. Vernizzi, M. Y. Lanzerotti, J. Kujawski, A. Weatherwax, "Topological Constraints for E. F. Rent's Work on Microminiature Packaging and Circuitry," IBM Jnl. Res. Dev., vol. 58, no. 2/3, pp. 13:1-17, Mar/May 2014.

[1]The views expressed in this article are those of the author and do not reflect the official policy or position of the United States Air Force, Department of Defense or the U.S. Government.

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