Characterization of structural defects in GST based nano-PCM devices through resistance drift measurements\textsuperscript{1} IBRAHIM CINAR, EGE-CAN COGULU, AISHA GOKCE, Bogazici University, BARRY STIPE, JORDAN KATINE, HGST, A Western Digital Company, GULEN AKTAS, OZHAN OZATAY, Bogazici University — Phase change memory (PCM) is a promising non-volatile data storage technology with its high signal to noise ratio and superior scalability. Resistance drift in amorphous phase of the phase change material poses a crucial reliability problem, especially in multiple-bit-per cell PCM devices. The resistance of the amorphous phase uncontrollably increases with time after a reset operation which alters the read/write conditions of the device. Structural relaxation (SR) through a defect annihilation process is considered to be the underlying physical mechanism for resistance drift. Here, we report on our measurements of the resistance drift in a phase change memory device with a single layer Ge\textsubscript{2}Sb\textsubscript{2}Te\textsubscript{5} (GST) material not only in the amorphous state but also in the intermediate resistance state in devices with square top contact geometry which enables us to assess the reliability of multiple-bit per cell PCM memory devices. Through an analysis of electrical measurements as a function of time and temperature for increasing annealing times, we estimate a rate of change in trap density for both amorphous and mixed phases of the GST material after a switching operation. Our study allows engineering the phase change materials and optimizing programing conditions for future PCM applications.

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Ibrahim Cinar
Bogazici University

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