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Performing repetitive error detection in a superconducting quantum circuit J. KELLY, UC Santa Barbara, R. BARENDS, A. FOWLER, Google, Santa Barbara, A. MEGRANT, UC Santa Barbara, E. JEFFREY, Google, Santa Barbara, T. WHITE, UC Santa Barbara, D. SANK, J. MUTUS, Google, Santa Barbara, B. CAMPBELL, UC Santa Barbara, Y. CHEN, Google, Santa Barbara, Z. CHEN, B. CHIARO, A. DUNSWORTH, I.-C. HOI, C. NEILL, P.J.J. O'MALLEY, UC Santa Barbara, P. ROUSHAN, Google, Santa Barbara, C. QUINTANA, A. VAINSENCHER, J. WENNER, A.N. CLELAND, UC Santa Barbara, J.M. MAR-TINIS, University of California and Google, Santa Barbara — Recently, there has been a large interest in the surface code error correction scheme, as gate and measurement fidelities are near the threshold. If error rates are sufficiently low, increased systems size leads to suppression of logical error. We have combined high fidelity gate and measurements in a single nine qubit device, and use it to perform up to eight rounds of repetitive bit error detection. We demonstrate suppression of environmentally-induced error as compared to a single physical qubit, as well as reduced logical error rates with increasing system size.

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