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**Quantifying Surface Loss Induced by Anti-Vortex Hole Arrays in Planar Superconducting Circuits for Quantum Computation** B. CHIARO, A. MEGRANT, A. DUNSWORTH, Z. CHEN, B. CAMPBELL, I.-C. HOI, J. KELLY, C. NEILL, P. J. J. O'MALLEY, C. QUINTANA, A. VAINSENCHER, J. WENNER, T. WHITE, UC Santa Barbara, R. BARENDS, Y. CHEN, A. FOWLER, E. JEFFREY, J. MUTUS, P. ROUSHAN, D. SANK, Google, Santa Barbara, A. N. CLELAND, UC Santa Barbara, J. M. MARTINIS, University of California and Google, Santa Barbara — Two important dissipation sources in superconducting circuits operated at low power are surface loss from two level systems (TLS) and magnetic vortex loss. By patterning the superconducting electrodes with an array of holes, it is possible to reduce or eliminate loss due to magnetic vortices. However, since the highest levels of coherence in planar superconducting circuits have been achieved by improving the electrode-substrate interface, it is natural to expect that adding hole arrays to the electrodes may cause excess surface loss. We present simulations predicting the excess loss magnitude to be $< 10\%$ for typical ground plane hole arrays, but for extreme cases of hole size or placement the loss may be much greater. We confirm the simulation result with measurements of high quality factor resonators ($Q_i > 10^6$) with and without the hole patterns.

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