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Ultra-low noise atomically patterned nanostructures in Si SAQUIB SHAMIM, Department of Physics, Indian Institute of Science, Bangalore 560012, India, BENT WEBER, MICHELLE Y. SIMMONS, Centre of Excellence for Quantum Computation and Communication Technology, University of New South WalesSydney, NSW 2052, Australia, ARINDAM GHOSH, Department of Physics, Indian Institute of Science, Bangalore 560012, India — Advancement in scanning tunnelling microscopy (STM) based lithography has made it possible to achieve low resistivity atomic scale wires and single donor quantum dot devices in silicon. Due to extreme sensitivity of these devices to any disorder or charge traps, it is of paramount importance to explore the noise magnitude in these systems. Here we investigate low frequency noise measurements in two STM patterned atomic scale wires of phosphorous dopants in Si of diameters 4.5 nm and 1.5 nm. The variation of noise with gate voltage indicates that the noise arises due to trapping-detrapping of electrons between the wire and charged traps. The Hooge parameter for these wires is 10^{-4} to 10^{-6} (for different gate voltages), which is one of the lowest reported for any one-dimensional system. The reason for such low noise magnitude can be two-fold. First, a complete monolithic fabrication procedure avoids any direct metallic contact to the one-dimensional system and hence prevents any Schottky barrier. Second possibility is that the Coulomb repulsion between the charges on traps doesn't allow many traps to be activated simultaneously. Aimed at being the backbone of silicon quantum computation scheme, a reduced noise in these devices is technologically crucial.

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