## Abstract Submitted for the MAR15 Meeting of The American Physical Society

Combination of conductance oscillation in the quantum Hall regime and charge trap flash memory phenomena in graphene field effect transistor YOOJOO YUN, HAEYONG KANG, JOONG-GYU KIM, JEONG-MIN PARK, THUY KIEU TRUONG, NAHEE PARK, JEONG-GYUN KIM, YOURACK LEE, CINAP, IBS, DOES, SungkyunKwan Univ., HOYEOL YUN, SANG WOOK LEE, School of Physics, Konkuk Univ., YOUNG HEE LEE, DONGSEOK SUH, CINAP, IBS, DOES, SungkyunKwan Univ., CINAP, IBS, DOES, SUNGKYUNKWAN UNIV. TEAM, SCHOOL OF PHYSICS, KONKUK UNIV. COLLABORATION — We present the feature of conductance oscillation in the quantum Hall regime graphene FET on top of large gate-voltage hysteresis (up to 100 V). A mono-layer graphene was put on the hBN flake on the wet silicon oxide/silicon substrate. At 300 K, the normal conductance versus gate-voltage curve was observed showing the charge neutrality point without hysteresis. At 2 K, however, there was a huge conductance hysteresis during the sweep of gate-voltage, which could be attributed to the characteristics of charge-trap memory behavior because of defects located inside the dielectric playing a role of charge-trap sites. Even though the hysteresis during gate-voltage sweeping was enormous, in our device having hBN for graphene device preventing the deteriorating impacts from the defective  $SiO_2$ , the conductance oscillation during the gate-voltage sweep was observed from the magnetic field 4 T. In summary, the results proved that the combination of quantum Hall related transport phenomena and the charge-trap memory operation was achieved successfully without affecting each other in our graphene-on-hBN FET device.

> Yoojoo Yun Sungkyunkwan Univ

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