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Rhenium Disulfide Depletion-Load Inverter[1] CONNOR MCCLELLAN, CHRIS CORBET, AMRITESH RAI, HEMA C.P. MOVVA, EMANUEL TUTUC, SANJAY K. BANERJEE, The University of Texas at Austin — Many semiconducting Transition Metal Dichalcogenide (TMD) materials have been effectively used to create Field-Effect Transistor (FET) devices but have yet to be used in logic designs. We constructed a depletion-load voltage inverter using ultrathin layers of Rhenium Disulfide (ReS_2) as the semiconducting channel. This ReS_2 inverter was fabricated on a single micromechanically-exfoliated flake of ReS_2. Electron beam lithography and physical vapor deposition were used to construct Cr/Au electrical contacts, an Alumina top-gate dielectric, and metal top-gate electrodes. By using both low (Aluminum) and high (Palladium) work-function metals as two separate top-gates on a single ReS_2 flake, we create a dual-gated depletion mode (D-mode) and enhancement mode (E-mode) FETs in series. Both FETs displayed current saturation in the output characteristics as a result of the FET "pinch-off" mechanism and On/Off current ratios of 10^5. Field-effect mobilities of 23 and 17 $cm^2V^{-1}s^{-1}$ and subthreshold swings of 97 and 551 mV/decade were calculated for the E-mode and D-mode FETs, respectively. With a supply voltage of 1V, at low/negative input voltages the inverter output was at a high logic state of 900 mV. Conversely with high/positive input voltages, the inverter output was at a low logic state of 500 mV. The inversion of the input signal demonstrates the potential for using ReS_2 in future integrated circuit designs and the versatility of depletion-load logic devices for TMD research.

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