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**Carbon nanotube high-performance logic technology – challenges and current progress**

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In the last four decades, we have witnessed a tremendous information technology revolution originated from the relentless scaling of Si complementary metal-oxide semiconductor (CMOS) devices. CMOS scaling provides ever-improved transistor performance, density, power and cost, and will continue to bring new applications and functions to our daily life. However, the conventional homogeneous scaling of silicon devices has become very difficult, firstly due to the unsatisfactory electrostatic control from the gate dielectric. In addition, as we look forward to the technology nodes with sub-10 nm channel length, non-Si based channel materials will be required to provide continuous carrier velocity enhancement when the conventional strained-Si techniques run out of steam. Single-walled carbon nanotubes are promising to replace silicon as the channel material for high-performance electronics near the end of silicon scaling roadmap, with their superb electrical properties, intrinsic ultrathin body, and nearly transparent contact with certain metals. This talk discusses recent advances in modeling and experimental works that reveal the properties and potential of ultra-scaled nanotube transistors, separation and assembly techniques for forming nanotube arrays with high semiconducting nanotube purity and tight pitch separation, and engineering aspects of their implementation in integrated circuits and functional systems. A concluding discussion highlights most significant challenges from technology points of view, and provides perspectives on the future of carbon nanotube based nanoelectronics.