Abstract Submitted
for the MAR16 Meeting of
The American Physical Society

**Towards a drift-free multi-level Phase Change Memory** IBRAHIM CINAR, Bogazici University, SERVET OZDEMIR, University of Warwick, EGECAN COGULU, New York University, AISHA GOKCE, Bogazici University, BARRY STIPE, JORDAN KATINE, HGST, A Western Digital Company, GULEN AKTAS, OZHAN OZATAY, Bogazici University — For ultra-high density data storage applications, Phase Change Memory (PCM) is considered a potentially disruptive technology. Yet, the long-term reliability of the logic levels corresponding to the resistance states of a PCM device is an important issue for a stable device operation since the resistance levels drift uncontrollably in time. The underlying mechanism for the resistance drift is considered as the structural relaxation and spontaneous crystallization at elevated temperatures. We fabricated a nanoscale single active layer-phase change memory cell with three resistance levels corresponding to crystalline, amorphous and intermediate states by controlling the current injection site geometry. For the intermediate state and the reset state, the activation energies and the trap distances have been found to be 0.021 eV and 0.235 eV, 1.31 nm and 7.56 nm, respectively. We attribute the ultra-low and weakly temperature dependent drift coefficient of the intermediate state ($\nu$ =0.0016) as opposed to that of the reset state ($\nu$ =0.077) as being due to the dominant contribution of the interfacial defects in electrical transport in the case of the mixed phase. Our results indicate that the engineering of interfacial defects will enable a drift-free multi-level PCM device design.

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Date submitted: 03 Nov 2015 Electronic form version 1.4