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**Interface investigation of solution processed high-$\kappa$ $ZrO_2$/Si MOS structure by DLTS** ARVIND KUMAR, SANDIP MONDAL, KSR KOTESWARA RAO, Dept of Physics, IISc, India — The interfacial region is dominating due to the continuous downscaling and integration of high-$k$ oxides in CMOS applications. The accurate characterization of high-$k$ oxides/semiconductor interface has the significant importance towards its usage in memory and thin film devices. The interface traps at the high$-k$/semiconductor interface can be quantified by deep level transient spectroscopy (DLTS) with better accuracy in contrast to capacitance-voltage (CV) and conductance technique. We report the fabrication of high-$k$ $ZrO_2$ films on p-Si substrate by a simple and inexpensive sol-gel spin-coating technique. Further, the $ZrO_2$/Si interface is characterized through DLTS. The flat-band voltage ($V_{FB}$) and the density of slow interface states (oxide trapped charges) extracted from CV characteristics are 0.37 V and 2x$10^{-11}$ C/cm$^2$, respectively. The activation energy, interface state density and capture cross-section quantified by DLTS are $E_V$+0.42 eV, 3.4x$10^{11}$ eV$^{-1}$ cm$^{-2}$ and 5.8x$10^{-18}$ cm$^2$, respectively. The high quality $ZrO_2$ films own high dielectric constant 15 with low leakage current density might be an appropriate insulating layer in future electronic application. The low value of interface state density and capture cross-section are the indication of high quality interface and the defect present at the interface may not affect the device performance to a great extent. The DLTS study provides a broad understanding about the traps present at the interface of spin-coated ZrO2/Si.

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