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Multi-Level Memory Effect of CVD Graphene Transferred on SiO_2 by Controlled Hydron Adsorption at Interface[1] SUNGCHUL JUNG, JUNHYOUNG KIM, HOON HAHN YOON, HAN BYUL JIN, GAHYUN CHOI, JUNG-YONG LEE, Ulsan Natl Inst of Sci Tech, DAEJIN EOM, Korea Research Institute of Standards and Science, KIBOG PARK, Ulsan Natl Inst of Sci Tech — Memory effect of graphene based on the Fermi-level shift driven by external electric field has been studied in various ways. There have been several experimental reports exploring the fabrication of two-level memory devices relying on the hysteresis loop of channel current vs. gate voltage of Graphene/SiO_2/Si field effect transistor (FET). This channel current hysteresis has been explained by the motion of the water molecules trapped between graphene and SiO_2 insulator. In this study, we fabricated a CVD-grown graphene FET on a SiO_2/Si substrate and found four different channel conductivity states tunable by varying the applied gate voltage pulse. It is noticed that the stabilization of reset state (lowest conductivity state) is one of the challenging issues in fabricating memory devices with graphene FET. We found that the stabilization of reset state can be achieved by positioning the Fermi-level in reset state as close to the charge neutrality point as possible during read-out. We propose one easy way to ensure the proper positioning of the reset state Fermi-level, which is to apply a constant gate voltage during read-out. Our study demonstrates the possibility of fabricating graphene-based multi-bit memory devices.

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