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Unconventional 1/f noise in Graphene on $SrTiO_3$ substrate ANINDITA SAHOO, Department of Physics, Indian Institute of Science, Bangalore-560012, India, ROALD RUITER, TAMALIKA BANERJEE, Zernike Institute for Advanced Materials, University of Groningen, Groningen, The Netherlands, ARINDAM GHOSH, Department of Physics, Indian Institute of Science, Bangalore-560012, India — Electrical transport in graphene has been of great interest in both fundamental and applied research. The impact of the substrate is critical to the operation of graphene field effect transistors (FET), which can modify several transport parameters as well as low frequency 1/f noise. Replacing the usual SiO_2/Si^{++} substrate with $SrTiO_3$ [STO] having high dielectric constant, has opened up new possibilities, leading to large doping, higher mobility, and also hysteretic transfer characteristics for memory applications. We have studied 1/f noise in dual-gated single layer graphene (SLG) FET sandwiched between STO (substrate) and mechanically exfoliated hexagonal boron-nitride (dielectric for the top gate). The area normalized noise amplitude of SLG on STO followed an unexpected 'W'-shape dependence of gate-bias with the central peak at Dirac point in conflict with the usual 'V', 'M' or 'Λ'-type dependence of SLG noise on SiO_2. We discuss possible microscopic mechanisms for such behavior, considering the role of puckering of oxygen atoms introducing inward dipole moments that can form a new source of electrostatically tunable scattering mechanism at the graphene-STO interface.

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