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Three-Dimensional Architecture at Chip Level for Large-Scale-Integration of Superconducting Quantum Electronic Devices MARTIN GÖPPL, Sensirion AG, PHILIPP KURPIERS, ANDREAS WALLRAFF, ETH Zurich — We propose a novel way to realize three-dimensional circuit QED systems at chip level. System components such as qubits, transmission lines, capacitors, inductors or cross-overs can be implemented as suspended, electromagnetically shielded and optionally, as hermetically sealed structures. Compared to known state-of-the-art devices, volumes of dielectrics penetrated by electromagnetic fields can be drastically reduced. Our intention is to harness process technologies for very-large-scale-integration, reliably applied and improved over decades in micro-sensor- and semiconductor industry, for the realization of highly integrated circuit QED systems. Process capabilities are demonstrated by fabricating first exploratory devices using the back-end-of-line part of a commercial 180 nm CMOS foundry process in conjunction with HF vapor phase release etching.

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