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Flexible, low-latency architecture for qubit control and measurement in circuit QED. WOUTER VLOTHUIZEN, D. DEURLOO, QuTech, Delft University of Technology and Netherlands Organisation for Applied Scientific Research (TNO), Delft, The Netherlands, J. DE STERKE, Topic Embedded Systems, Delft, The Netherlands, R. VERMEULEN, R.N. SCHOUTEN, LEO DICARLO, QuTech and Kavli Institute of Nanoscience, Delft University of Technology, Delft, The Netherlands — Increasing qubit numbers in circuit QED requires an extensible architecture for digital waveform generation of qubit control and measurement signals. For quantum error correction, the ability to select from a number of predetermined waveforms based on measurement results will become paramount. We present a room-temperature architecture with very low latency from measurement to waveform output. This modular FPGA-based system can generate both baseband and RF modulated signals using DACs clocked at 1 GHz. A backplane that interconnects several modules allows exchange of (measurement) information between modules and maintains deterministic timing across those modules. We replace the typical line based sequencer used in arbitrary waveform generators by a user programmable processor that treats waveforms and measurements as instructions added to a conventional CPU architecture. This allows for flexible coding of triggering, repetitions, delays and interactions between measurement and signal generation. We acknowledge funding from the Dutch Research Organization (NWO), an ERC Synergy Grant, and European project SCALEQIT.

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