Abstract Submitted
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Assessing MOS Interface Quality for Silicon Quantum Dot Device Fabrication RYAN STEIN, Joint Quantum Institute, University of Maryland, JIN-SUNG KIM, STEVE LYON, Department of Electrical Engineering, Princeton University, NEIL M. ZIMMERMAN, M. D. STEWART, JR., National Institute of Standards and Technology — Defects at the Si-SiO2 interface are capable of trapping electrons and degrading the operation of silicon-based quantum dot devices. To improve device performance, we are working to characterize the interface quality in MOSCAPs and MOSFETs fabricated at NIST by comparing industry standard defect measurements, such as capacitance-voltage (CV), conductance, and mobility, to electron spin resonance (ESR) measurements. This comparison will give insight into the relative role of defects near the band edge and those distributed throughout the gap in degrading device performance. We will discuss our progress toward this goal as well as our latest data and interpretations.

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