Abstract Submitted
for the MAR16 Meeting of
The American Physical Society

Vertical gating of sketched nanodevices[1] YUN-YI PAI, University of Pittsburgh, DONG-WOOK PARK, University of Wisconsin at Madison, MENGCHEN HUANG, ANIL ANNADI, University of Pittsburgh, HYUNGWOO LEE, ZHENQIANG MA, CHANG-BEOM EOM, University of Wisconsin at Madison, PATRICK IRVIN, JEREMY LEVY, University of Pittsburgh — Conductive-atomic force microscope (c-AFM) lithography at the $LaAlO_3/SrTiO_3$ interface has enabled the creation of various classes of nanostructures, such as nanoscale transistors[2], single-electron transistors[3] and has proven to be a promising testbed for mesoscopic physics[4]. To date, these devices have used lithographically-defined side gates, which are limited by leakage currents. To reduce leakage and improve the electric field effect, we have investigated nanostructures with in-situ grown gold top gate. We will discuss designs of logic devices such as inverters, NAND, and NOR gates. In the quantum regime, we compare the performance of in-situ vertical top gates and that of written coplanar side gates with Quantum Dot devices.

[1]We gratefully acknowledge financial support from the following agencies and grants: AFOSR (FA9550-10-1-0524(JL), FA9550-12-1-0342(CBE)), NSF (DMR1124131 (JL, CBE) and DMR1234096 (CBE)), ONR (N00014-15-1-2847 (JL)).
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Date submitted: 06 Nov 2015 Electronic form version 1.4