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Toward spin-based Magneto Logic Gate in Graphene HUA WEN, Dept of Physics and Astronomy, Univ. of California, Riverside, HANAN DERY, Dept. of Electrical and Computer Engineering, University of Rochester, WALID AMAMOU, Dept. of Physics and Astronomy, University of California, Riverside, TIANCONG ZHU, Dept. of Physics, The Ohio State University, ZHISHENG LIN, Deptt. of Physics and Astronomy, University of California, Riverside, JING SHI, Dept. of Physics and Astronomy, University of California, Riverside, IGOR ZUTIC, Dept. of Physics, University at Buffalo, State University of New York, ILYA KRIVOROTOV, Dept. of Physics and Astronomy, University of California, Irvine, LU SHAM, Dept. of Physics, University of California, San Diego, ROLAND KAWAKAMI, Dept. of Physics, The Ohio State University — Graphene has emerged as a leading candidate for spintronic applications due to its long spin diffusion length at room temperature. A universal magnetologic gate (MLG) based on spin transport in graphene has been recently proposed as the building block of a logic circuit which could replace the current CMOS technology. This MLG has five ferromagnetic electrodes contacting a graphene channel and can be considered as two three-terminal XOR logic gates. Here we demonstrate this XOR logic gate operation in such a device. This was achieved by systematically tuning the injection current bias to balance the spin polarization efficiency of the two inputs, and offset voltage in the detection circuit to obtain binary outputs. The output is a current which corresponds to different logic states: zero current is logic '0', and nonzero current is logic '1'. We find improved performance could be achieved by reducing device size and optimizing the contacts.

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