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Comparison of charge offset drift in Si/SiO_2 based single electron devices of differing geometry BINHUI HU, University of Maryland-College Park, NEIL M. ZIMMERMAN, M. D. STEWART, JR., National Institute of Standards and Technology — Practical applications of single electron devices (SEDs) require that each SED is stable during operation. However, a low-frequency time instability known as charge offset drift is present in real SEDs. Experimentally, it is well established that the charge offset drift is large in Al/AlO_x based SEDs (ΔQ_0>1e) and minimal in mesa-etched Si/SiO_2 based silicon on insulator (SOI) devices (ΔQ_0<0.01e) [1]. This result has been interpreted to be a consequence of intrinsic material properties. Specifically, the level of interaction between TLS defects present in the amorphous insulators, AlO_x and SiO_2, is distinctly different [1]. We will present recent measurements on Si/SiO_2-based single-layer SEDs fabricated on bulk wafers which show appreciable charge offset drift, in discrepancy with the above interpretation. We will discuss these results in the context of the origin of charge offset drift in the Si/SiO_2 material system and the role being played by device structure. [1] M. D. Stewart, Jr. and Neil M. Zimmerman, Appl. Sci. 2016, 6(7), 187, and references therein.

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