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### **Passive Error Correction and Gates for a Very Small Logical Qubit**

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In this talk, I discuss further theoretical developments of the proposed "Very Small Logical Qubit" architecture, which promises order-of-magnitude coherence increases over any of its component parts for T1 and T2 values commonly achieved in experiments. These improvements come from engineered dissipation and do not require active measurement or intervention. However, to be useful for constructing a quantum computer, gate error must be reduced as well. To do so, I propose a realistic implementation of a universal one- and two-qubit gate set for the VSLQ, with finely tuned gate operations that are resilient to random errors which occur mid-gate. I numerically benchmark the operations to demonstrate improved gate fidelity, with superlinear reduction in gate error with linear increase in T1. These results suggest that small logical qubits could be integrated into a measurement-based code for improved error correction performance.