Abstract Submitted
for the MAR17 Meeting of
The American Physical Society

Silicon Hard-Stop Mesas for 3D Integration of Superconducting Qubits DAVID KIM, DANNA ROSENBERG, BRENDA OSADCHY, GREG CALUSINE, RABINDRA DAS, ALEXANDER MELVILLE, JONILYN YODER, DONNA-RUTH YOST, LIVIA RACZ, MIT Lincoln Laboratory, WILLIAM OLIVER, MIT Lincoln Laboratory; Research Laboratory of Electronics, MIT — As quantum computing with superconducting qubits advances past the few-qubit stage, implementing 3D packaging/integration to route readout/control lines will become increasingly important. One approach is to bond chips that perform different functions using indium bump bonds. Because indium is malleable, however, achieving the desired spacing and tilt between two chips can be challenging. We present an approach based on etching several microns into the silicon substrate to produce hard stop silicon posts. Since this process involves etching into a pristine substrate, it is essential to evaluate its impact on qubit performance. We report the etched surface's effect on the resonator quality factor and qubit coherence time, as well as the improvement in planarity and tilt. This research was funded in part by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA) and by the Assistant Secretary of Defense for Research & Engineering under Air Force Contract No. FA8721-05-C-0002. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of ODNI, IARPA, or the US Government.

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Date submitted: 10 Nov 2016 Electronic form version 1.4