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Testing of a bottom-up approach for electrically contacting nanoscale quantum electronic devices ARUNA RAMANAYAKA, National Institute of Standards and Technology, HYUN-SOO KIM, KE TANG, University of Maryland, National Institute of Standards and Technology, M. D. STEWART, JR., J. M. POMEROY, National Institute of Standards and Technology — We present a complementary metal–oxide–semiconductor (CMOS) technology compatible bottom-up approach for realizing electrical connections to nanoscale quantum electronic devices. State of the art fabrication methods used for making external electrical contacts to nanoscale devices utilizes complex, time consuming, and expensive fabrication techniques. In order to simplify the fabrication of these electrical contacts, we create pre-pattered electrical contact wires that are degenerately doped regions in the substrate and extend down to micrometer scale using photolithography and low energy ion implantation. With this approach we are able not only to bring external electrical contacts close to a single field of view of a scanning tunneling microscope (STM), approximately 10 m x 10 m area, allowing the STM to draw direct electrical connections between these external electrical lines and the nanoscale device, but also to cut down the fabrication time considerably by fabricating pre-patterned electrical contacts at wafer scale. However, proximity of these implant lines has to be restricted due to the diffusion of implanted ions during high temperature processing of Si substrates, e.g., substrate preparation, implant activation, and oxidation. We will discuss the limitations for different high temperature processing methods, and electrical measurements of a nanoscale device using pre-defined external contacts.

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