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Quantum Conductance of Graphene Field Effect Transistor on $SrTiO_3$ Epitaxial Thin Film[1] JEONGMIN PARK, CINAP, IBS, DOES, SKKU, Suwon 16419, Korea, HAEYONG KANG, DOES, SKKU, Suwon 16419, Korea, KYEONG TAE KANG, Department of Physics, SKKU, Suwon 16419, Korea, YOO-JOO YUN, YOUNG HEE LEE, CINAP, IBS, DOES, SKKU, Suwon 16419, Korea, WOO SEOK CHOI, Department of Physics, SKKU, Suwon 16419, Korea, DONGSEOK SUH, CINAP, IBS, DOES, SKKU, Suwon 16419, Korea — In this work [1], graphene field effect transistor (FET) combined with epitaxial $SrTiO_3$ (STO) thin film of ultrahigh-k dielectric constant, was examined to check the possibility of gate-voltage scaling. Due to the atomically flat surface of thin STO film grown on Nb-doped STO single-crystal substrate, the interface between graphene and STO showed good adhesion and nonhysteretic electrical conduction as function of gate bias was observed in all temperature ranges down to 2 K. Furthermore, quantized conductance corresponding to quantum Hall state was observed up to 200 K in a magnetic field of 14 T. We noticed that the temperature-dependent shift of charge neutrality point in graphene FET is correlated with the STO's dielectric constant variation. In addition, from the analysis of the universality of quantum phenomena in graphene, effective dielectric properties of STO thin film could be deduced. Our results indicate that operating gate bias was reduced successfully by using high-k STO thin film as gate insulator, without any drawback of graphene FET performance. [1] J. Park et. al., Nano Lett., 2016, 16 (3), pp 1754–1759

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