Optimization of passive error correction parameters for the Very Small Logical Qubit

DAVID RODRIGUEZ PEREZ, Tulane University, ERIC HOLLAND, JONATHAN DUBOIS, Lawrence Livermore National Laboratory, ELIOT KAPIT, Tulane University — The Very Small Logical Qubit is a promising route to passive error correction in superconducting qubit architectures. However; optimal circuit parameters for given single qubit lifetimes and nonlinearities are not yet known. We describe a numerical optimization scheme to find the optimal device and signal parameters to maximize the logical state lifetime in simulations with realistic single qubit error rates, and report theoretical coherence times $T_L$ exceeding 1 ms for single qubit $T_1$ as low as 20 $\mu$s. These results clearly illustrate the tradeoff between rapid error correction and noise induced by the error correction mechanism itself. Further, we consider higher order corrections beyond the three-level approximation, and show that their effects can be easily mitigated.