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Optimizing gates in the presence of leakage errors[1] CHRISTOPHER J. WOOD, DAVID C. MCKAY, SARAH SHELDON, JERRY M. CHOW, JAY M. GAMBETTA, IBM T J Watson Res Ctr — As coherence times of superconducting transmon qubits improve, leakage errors become an important error source that must be taken into account for the design of high fidelity gates, and for achieving fault tolerance thresholds in surface code protocols. We discuss methods for quantifying and characterizing leakage errors in quantum gates, and show how these relate to standard measures of average gate fidelity from randomized benchmarking. We also compare methods for achieving low-leakage, high fidelity single qubit gates by using alternative techniques to standard DRAG control pulses.

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Christopher J. Wood
IBM T J Watson Res Ctr

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