Abstract Submitted
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High Coherence Qubit packaging[1] DAVID P. PAPPAS, XIAN WU, NIST - Boulder, SALVATORE B. OLIVADESE, V. P. ADIGA, JARED B. HERTZBERG, NICHOLAS T. BRONN, JERRY M. CHOW, IBM, NIST TEAM, IBM TEAM — Development of sockets and associated interconnects for multi-qubit chips is presented. Considerations include thermalization, RF hygiene, non-magnetic environment, and self-alignment of the chips to allow for rapid testing, scalable integration, and high coherence operation. The sockets include wirebond free, vertical take-off launches with pogopins. This allows for high interconnectivity to non-trivial topology of qubits. Furthermore, vertical grounding is accomplished to reduce chip modes and suppress box modes. Low energy loss and high phase coherence is observed using this paradigm.

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