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Fabrication of Circuit QED Quantum Processors, Part 1: Extensible Footprint for a Superconducting Surface Code[1] A. BRUNO, QuTech and Kavli Institute of Nanoscience, Delft University of Technology, The Netherlands, D.J. MICHALAK, Intel Corporation, USA, S. POLETTO , QuTech and Kavli Institute of Nanoscience, Delft University of Technology, The Netherlands, J.S. CLARKE, Intel Corporation, USA, L. DICARLO, QuTech and Kavli Institute of Nanoscience, Delft University of Technology, The Netherlands — Large-scale quantum computation hinges on the ability to preserve and process quantum information with higher fidelity by increasing redundancy in a quantum error correction code. We present the realization of a scalable footprint for superconducting surface code based on planar circuit QED. We developed a tileable unit cell for surface code with all I/O routed vertically by means of superconducting through-silicon vias (TSVs). We address some of the challenges encountered during the fabrication and assembly of these chips, such as the quality of etch of the TSV, the uniformity of the ALD TiN coating conformal to the TSV, and the reliability of superconducting indium contact between the chips and PCB. We compare measured performance to a detailed list of specifications required for the realization of quantum fault tolerance. Our demonstration using centimeter-scale chips can accommodate the ˜50 qubits needed to target the experimental demonstration of small-distance logical qubits.

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