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Gate-tuned Longitudinal Spin Seebeck Effect in Topological Insulators¹ VICTOR H. ORTIZ, YADONG XU, MOHAMMED ALDOSARY, Department of Physics and Astronomy, University of California, Riverside, CUI-ZU CHANG, Francis Bitter Magnet Lab, Massachusetts Institute of Technology, JING SHI, Department of Physics and Astronomy, University of California, Riverside — The recent study of the topological spin Seebeck effect (SSE) in magnetic insulator (MI)/topological insulator (TI) heterostructures has raised an interesting question about the Fermi level tuning in the topological surface states of the TI and its effects on the spin Seebeck voltage (V_{SSE}) . In this work, we fabricate longitudinal SSE devices with a 50 nm Al_2O_3 layer prepared by a two-step atomic layer deposition process. In this structure, the heater atop Al_2O_3 serves as a top gate as well. The MI/TI heterostructure samples consist of a 20 nm YIG and a 5 quintuple layer thick $(\text{Bi}_{1-x}\text{Sb}_x)_2\text{Te}_3$ (x = 0.25, 0.27, 0.30 and 0.32) TI thin film. As the top gate voltage is swept, the resistance of the TI sample shows expected changes as the Fermi level position is varied. However, as the heater is turned on to measure the SSE response while the gate voltage is simultaneously swept, we find that the V_{SSE}/R ratio does not show a significant variation despite the observed change in resistance. We attribute this effect to the insensitivity of the bottom TI surface to top gate voltage. This result also suggests a short spin diffusion length in TI.

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