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The Analog Information Limit of Magnetic Domain Wall Positions in Nanowires SUMIT DUTTA, SAIMA SIDDIQUI, JOSEPH FINLEY, CAROLINE ROSS, MARC BALDO, Massachusetts Institute of Technology — Nonvolatile memory and logic devices are often made of magnetic nanowires with mobile domain walls (DWs). When the wire width is scaled to below 100 nm, the line edge roughness (LER) plays a larger role in domain wall dynamics. We explain how discrete domain wall pinning sites are distributed in sub-100-nm-wide wires with LER. Based on measurements of 60-nm-wide Co wires and micromagnetic modeling of DW motion and pinning in such wires, we understand LER-influenced trap distributions and their effects on the information density and control in DW memory and logic applications such as racetrack memory.

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