MAR17-2016-020332

Abstract for an Invited Paper
for the MAR17 Meeting of
the American Physical Society

An extensible circuit QED architecture for quantum computation[1]

LEO DICARLO, QuTech and Kavli Institute of Nanoscience, Delft University of Technology and Intel Corporation

Realizing a logical qubit robust to single errors in its constituent physical elements is an immediate challenge for quantum information processing platforms. A longer-term challenge will be achieving quantum fault tolerance, i.e., improving logical qubit resilience by increasing redundancy in the underlying quantum error correction code (QEC). In QuTech, we target these challenges in collaboration with industrial and academic partners. I will present the circuit QED quantum hardware, room-temperature control electronics, and software components of the complete architecture. I will show the extensibility of each component to the Surface-17 and -49 circuits needed to reach the objectives with surface-code QEC, and provide an overview of latest developments.

[1]Research funded by IARPA and Intel Corporation.