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Understanding the physics that causes hysteresis in carbon nanotube transistors, a key step toward high performance and energy-efficiency

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Three-dimensional (3D) integration is a promising technology that achieves higher energy efficiency, higher performance, and smaller footprint than today's planar, 2D technology [1]. In particular, carbon nanotube field-effect transistors (CNFETs) enable monolithic 3D integration due to its low-temperature processing (<400 C) [2]. Although CNFETs promise high-performance and energy-efficient digital systems, large hysteresis has long remained a challenge. Our approach to eliminating hysteresis is based on our understanding of the physics that lead to hysteresis [3]:

Understanding the sources of hysteresis: We develop a novel measurement technique called the Pulsed Time-Domain Measurement (PTDM) which enables quantification of charged traps responsible for hysteresis. Leveraging a physics-based model, we study the mechanism of the charge trapping process.

Eliminating hysteresis: After gaining a deeper understanding of the sources of hysteresis, we are able to develop a VLSI-compatible, solid-state fabrication method that mitigates the effect of traps. On average, we achieve hysteresis of less than 0.5% of the gate-source voltage sweep range.

Reference:

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