MAR17-2017-020734

Abstract for an Invited Paper
for the MAR17 Meeting of
the American Physical Society

David Adler Lectureship Award Talk: III-V Semiconductor Nanowires on Silicon for Future Devices.

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Bottom-up grown nanowires are very attractive materials for direct integration of III-V semiconductors on silicon thus opening up new possibilities for the design and fabrication of nanoscale devices for electronic, optoelectronic as well as quantum information applications. Template-Assisted Selective Epitaxy (TASE) allows the well-defined and monolithic integration of complex III-V nanostructures and devices on silicon. Achieving atomically abrupt heterointerfaces, high crystal quality and control of dimension down to 1D nanowires enabled the demonstration of FETs and tunnel devices based on In(Ga)As and GaSb. Furthermore, the strong influence of strain on nanowires as well as results on quantum transport studies of InAs nanowires with well-defined geometry will be presented.