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The effect of oxide impurities on the performance of 4H-SiC MOSFETs[1] XINGGUANG ZHU, A.C. AHYI, J.R. WILLIAMS, 206 Allison Lab, Auburn University, Auburn, AL 36849 — Recent studies for SiC [1] show that oxidation in the presence of metal impurities (especially Na) introduced from an alumina environment yields enhanced thermal oxidation rate, low interface trap density, and high MOSFET channel mobility. In this work, different sodium compounds (NaCl, Na_2O_2) and ion implantation were used to introduce Na at different stages during the oxidation process. The effect on oxide growth rate is discussed and interface trap densities are reported for simultaneous hi-lo C-V measurements using n-4H-MOS capacitors. Positive Bias Temperature Stress (1.5MV/cm, 5min, 250^{o}C) to move the mobile ions to the SiO_2/SiC interface produced a significant increase in MOSFET channel mobility, while no such effect was observed for Negative BTS. This indicates the possibility of a shielding mechanism for negatively charged interface traps when positive mobile ions are present at the oxide-semiconductor interface. [1] F. Allerstam, *et al.*, J. Appl. Phys. **101** (2007) 124502.

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