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Capturing Ion-Solid Interactions with MOS structures R. SHYAM, D.A. FIELD, Dept. of Physics and Astronomy, Clemson University, S. CHAMBERS, W.R. HARRELL, Dept. of Electrical and Computer Engineering,Clemson University, C.E. SOSOLIK, Dept. of Physics and Astronomy, Clemson University —
We have fabricated metal-oxide-semiconductor (MOS) devices for a study of implantation rates and damage resulting from low energy ion-solid impacts. Specifically, we seek to capture ion irradiation effects on the oxides. Fabrication of the MOS devices follows a standard procedure where Ohmic contacts are first created on the wafer backside followed by the thermal growth of various thicknesses of SiO_2 (from 50 nm to 200 nm) on the wafer frontside. As-grown SiO_2 layers are then exposed to various singly-charged alkalis ions with energies in the range of 100 eV to 10 keV in our beamline setup. Following this exposure, the MOS devices are completed in situ with the deposition of a top Al contact. Characterization of the ion-modified devices involves the standard device technique of biased capacitance-voltage (C-V) measurements where a field is applied across the MOS structure at an elevated temperature to move implanted ions resulting in changes in surface charge density that are reflected as shifts in the flatband voltage (V_{FB}). Similarly, a triangular voltage sweep (TVS) test can be utilized to measure the ionic displacement current as it is driven by a slow linear voltage ramp and it should reveal the total ionic space charge in an MOS.

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