Abstract Submitted
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Quantifying the Risk of Damage to Integrated circuits to Space Radiation and Mitigation Methods WILLIAM ATKINSON[1], Boeing Company, SPACE RADIATION EFFECTS TEAM[2] — The risk that electronics face in space from energetic charged particles emitted by the sun can be large. The risk varies from transient Single Event Upsets (SEUs) to permanent damage in Single Event Burnouts (SEBs). All of these single event effects are produced by an energetic particle striking a transistor. In space the particle may be a proton, alpha particle, or an ion as heavy as iron. In the atmosphere, the offending particle is a neutron produced by cosmic ray reacting at the nuclear level with air molecules. This presentation discusses software analysis tools designed to help quantify the risk space weather can pose to electronics and methods to mitigate the risk to the electronics. One such tool is TSAREME (Total Space and Atmospheric Radiation Effects on Microelectronics).The TSAREME results shown agree well with satellite measurements taken over four years for various integrated Circuit (IC) designs with feature sizes varying from a couple of microns to 15 nanometers. Major findings using TSAREME were that there are a number of alternatives to conventional CMOS ICs that significantly reduce the risk of electronic disruptions in space. Among these alternatives are silicon-on-insulator, and silicon-on-sapphire.

[1]This is for a plenary presentation.
[2]N/A

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