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**Electronic structure and Schottky-barrier height of Si/PtSi interface**
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With the use of silicides in CMOS devices, the sheet and contact resistances in source/drain regions are greatly reduced, which eventually causes the device speed increase. However, for the ultra-scaled devices, the serial contact resistance coming from relatively high Schottky-barrier between Si in the source/drain regions and the metallic contact is expected to amount to one-fourth of the total parasitic resistance. This contribution will clearly only rise as the scaling continues. Over the past two decades, Titanium disilicide ($TiSi_2$) has become the preferred silicide in integrated circuit manufacturing. However, the sheet resistance of $TiSi_2$ increases significantly as one of the device dimensions is reduced. In deep submicron regime, PtSi and NiSi have been shown to be prospective candidates for replacing conventional silicides. PtSi has relatively low Schottky-barrier on Si (001) and its structural and electronic properties are less sensitive to lateral dimensions. We have performed density functional calculations of work functions and surface energies of PtSi for different surface orientations and calculated Schottky-barrier height of Si/PtSi interface. We have also studied the effects of Boron doping in PtSi on its electronic structure and Si/PtSi Schottky-barrier. Our results are consistent with the existing experimental results. Finally, we discuss how Boron doping in PtSi may improve its metallic character and influence Si/PtSi Schottky-barrier height.

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