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Development of Etch Processes for High-k Dielectric CMOS Devices with LaO_x/HfO_2 and LaO_x/HfSiO Gate Oxides KELLY RADER, CARL VENTRICE, Dept. of Physics, Texas State University, PATRICK LYSAGHT, SEMATECH — High-k dielectric CMOS devices for low standby power applications require a low workfunction oxide on the n-MOSFET side of the CMOS device to reduce the threshold voltage and gate leakage. A promising candidate for this application is LaO_x. However, a process for etching the LaO_x from the p-MOSFET, which leaves the n-side intact, is required. A wet etch study, which enables the creation of a simplified process flow for CMOS devices using LaO_x on the n-side intact, is presented. The oxidation states and stoichiometry of the LaO_x films is investigated via x-ray photoelectron spectroscopy (XPS).

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