

Abstract Submitted
for the APR18 Meeting of
The American Physical Society

ASICs for FRIB DANIEL HOFF, JON ELSON, LEE SOBOTKA, Washington University in St. Louis, GEORGE ENGEL, Southern Illinois University Edwardsville — Historically, analog signal processing systems have been large and cumbersome, but the production of ASICs for analog signal processing has proved to be a cost-effective solution for creating large channel-count (100s and up) detector systems. Aside from those for TPCs, the SIUE-WUSTL effort, reviewed in this talk, is the sole effort in the US invested in making ASICs for use at FRIB. Two new versions of existing chips and one new chip are currently under design and/or production. The most recent HINP ASIC, widely used for modest-to-large arrays of Si detectors, provides two active gain ranges but does not allow an external charge-sensitive (pre)amplifier (unlike the previous version). The next version will return the external CSA option, retain the dual-gain shapers and be compatible with a dual-gain CSA ASIC designed at RIKEN. A second, and greatly improved, PSD ASIC with three gated integrators per channel - has been designed and fabricated and the support electronics are currently being upgraded. A 16-ch CFD ASIC has been designed and will be fabricated in 2018. The PSD+CFD chips are designed to work together to allow for large channel count arrays of scintillators with n/γ or charged-particle differentiable signal forms.

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Date submitted: 18 Jan 2018

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