Abstract Submitted
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Exploring High AR 2μm TSV (25:1) MAARTEN KOSTERMANS, ULRICH BAIER, WERNER BOULLART, imec, MOHAND BROURI, JOHAN VERTOMMEN, Lam, ARNAUD PAGEAU, Polytech Orleans — 3D integration allows for reduction of the system size, both in area and volume. It improves performance since 3D interconnects are shorter than traditional interconnects in a 2D configuration, enabling a higher operation speed and smaller power consumption. In order to ensure a reliable pattern transfer, a basic requirement for the etch mechanism is to provide anisotropy. Traditionally, through-silicon vias (TSVs) are achieved by means of the Bosch process, where anisotropic etch occurs via cycles of deposition and etch steps. This work investigates the etch process for 2 μm diameter vias with an aspect ratio up to 25:1, by means of an industrial ICP etch chamber with pulsed low frequency bias and ramping of different parameters like gasflows, bias voltage and separate etch and deposition step times. In order to reduce bowing while maintaining acceptable top/bottom CDs and reduce sidewall roughness, mechanisms of sidewall passivation have been studied by changing bias power duty cycle, modifying gas flow ramps, and O2 addition. Finally, scaling rules have been established that allow to predict etch time for various TSV diameters and A/R.

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